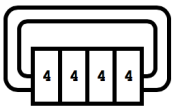
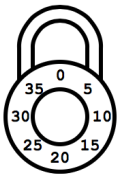
Sequential Logic

Learning Objectives

1. State the difference between combinational and sequential logic.
2. Identify rising and falling edges of a signal.
3. State the difference between edge triggered and level triggered circuit.
4. Complete timing diagrams for an SR latch, D latch, and D flip-flop.

Combinational versus Sequential

There are two types of locks:

_____:	 	_____:
Depends only on _____, not the _____ in which they were set		Depends on the input _____

_____ always give the same output for a given set of inputs

ex/ _____

_____ depend on the current state and the input. Therefore, these circuits have _____. They are used to _____

ex/ _____

S_____ R_____ (S-R) Latch

Latches are _____ devices. They are _____ sensitive.

_____ sensitive: the output changes when the value of the input changes.

_____ - value of Q becomes _____, regardless of previous value

_____ - value of Q becomes _____, regardless of previous value

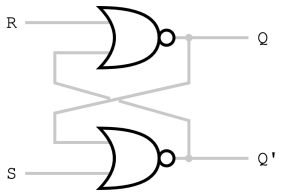
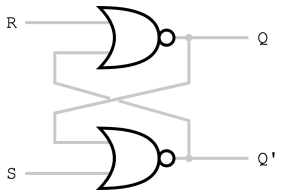
This logic circuit has two versions: active _____ and active _____.

Active _____

Review - Nor Truth Table

Symbol & Truth Table	If one of the inputs of a nor gate is 1, the output must be _____

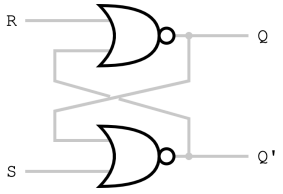
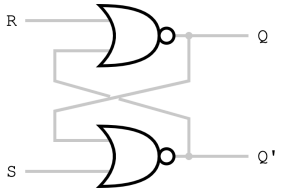
Reset and Set Conditions

reset: S = 0, R = 1  	If R = 1, Q "resets" to _____ Since Q is _____ and S is 0, Q' becomes _____
set: S = 1, R = 0  	If S = 1, Q' becomes _____ Since Q' is _____ and R is 0, Q is "set" to _____

Hold Condition, R = S = 0

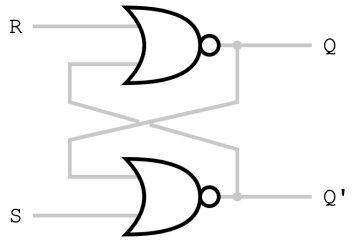
We can't predict the output of a nor gate if we know only one of the inputs is _____.

So for S = R = 0, we must know the initial values of Q & Q' to determine the outputs.

S = R = 0, Q_init = 0, Q'_init = 1  	If Q is initially 0 and Q' is initially 1, then the output of the _____ nor gate stays _____, and the output of the other nand gate stays _____.
S = R = 0, Q_init = 1, Q'_init = 0  	If Q is initially 1 and Q' is initially 0, then the output of the _____ nor gate stays _____, and the output of the other nand gate stays _____.

Invalid Input Combination: S = R = 1

Problem 1: Conflict

S = 1, R = 1  	If both S and R are equal to 1, then both Q and Q' will want to be _____. This creates a _____.

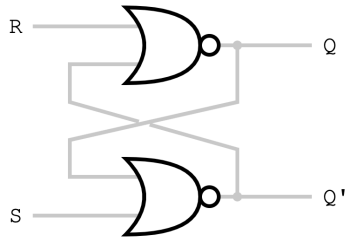
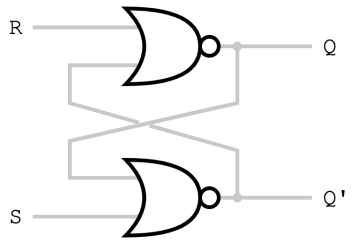
Problem 2: Race Condition

The final values of Q and Q' are _____ when changing from

_____ to _____.

The _____ for a signal to travel through a wire is _____.

So, we cannot assume two signals can change at precisely the same time.

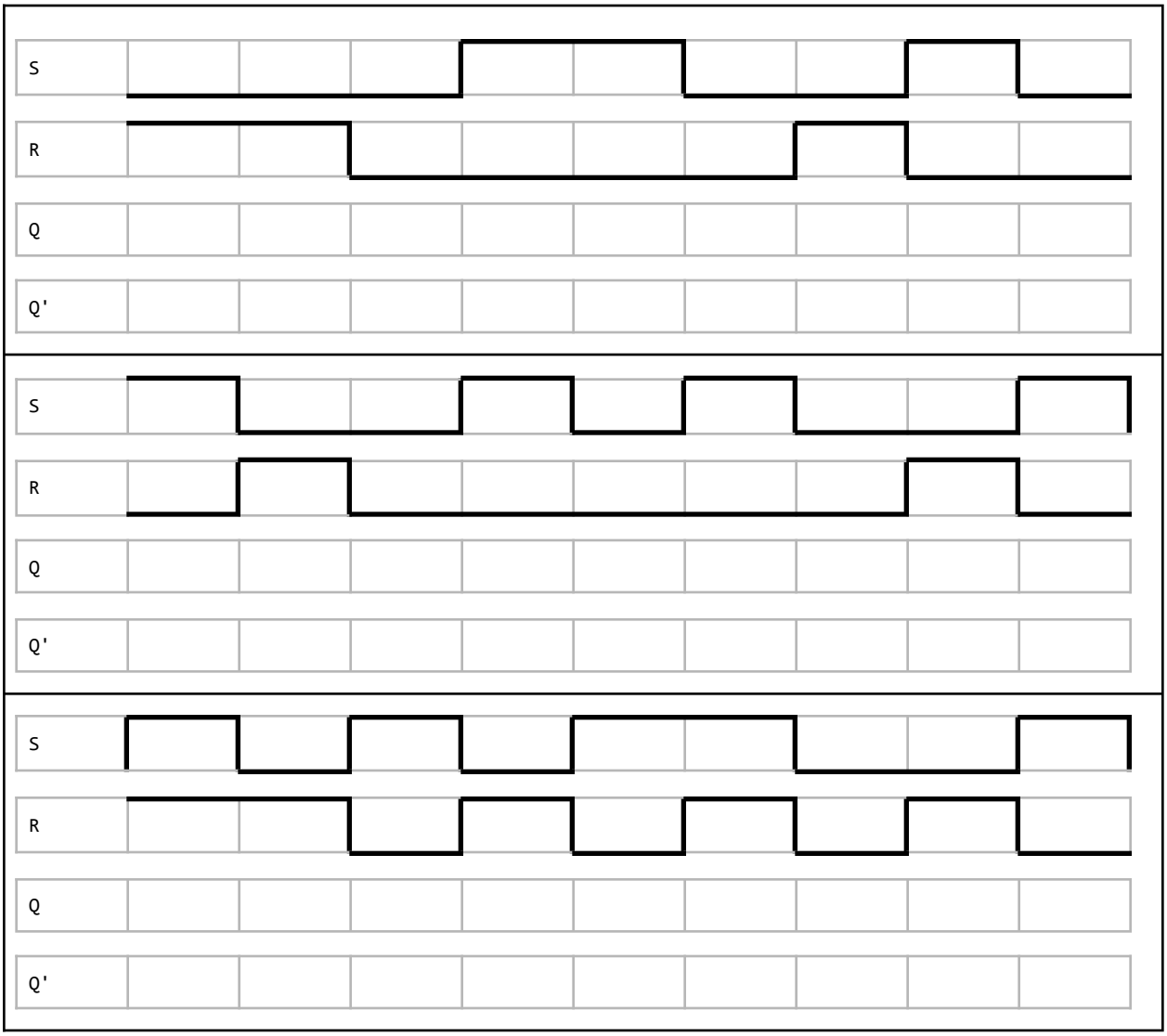
S = R = 0; Q_init = Q'_init = 0; R changes first  	If R changes from 1 to 0 first, Q will become _____ which will cause Q' to become _____
S = R = 0; Q_init = Q'_init = 0; S changes first  	If S changes from 1 to 0 first, Q' will become _____ which will cause Q to become _____

Summary

S	R	Q	Q'	Action
0	0			
0	1			
1	0			
1	1			

Active _____ S-R Latch Timing Diagrams

Fill out Q and Q' for given S and R signals.

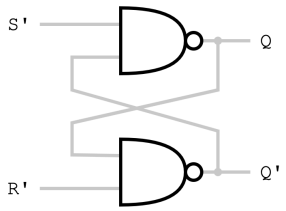
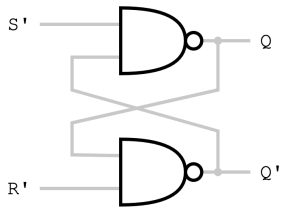


Active _____

Review - Nand Truth Table

Symbol & Truth Table	If one of the inputs is 0, the output must be _____

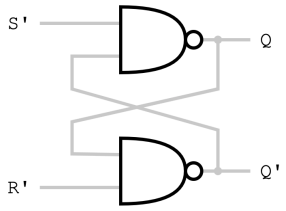
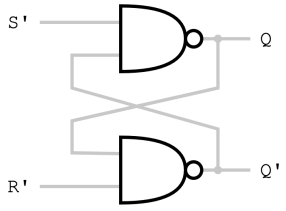
Reset and Set Conditions

set: S' = 0, R' = 1  	If S' = 0, Q is "set" to _____ Since Q is _____ and R' is 1, Q' becomes _____
reset: S' = 1, R' = 0  	If R' = 0, Q' becomes _____ Since Q' is _____ and S' is 1, Q is “reset” to _____

Hold Condition, R' = S' = 1

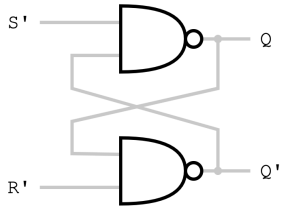
We can't predict the output of a nand gate if we know only one of the inputs is ____.

So for S'= R'= 1, we must know the initial values of Q & Q' to determine the outputs.

S' = R' = 1, Q_init = 0, Q'_init = 1  	If Q is initially 0 and Q' is initially 1, then the output of the _____ nand gate stays _____, and the output of the other nand gate stays _____.
S' = R' = 1, Q_init = 1, Q'_init = 0  	If Q is initially 1 and Q' is initially 0, then the output of the _____ nand gate stays _____, and the output of the other nand gate stays _____.

Invalid Input Combination: S' = R' = 0

Problem 1: Conflict

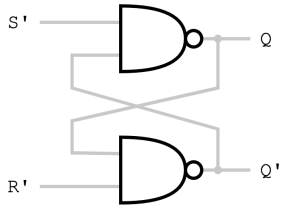
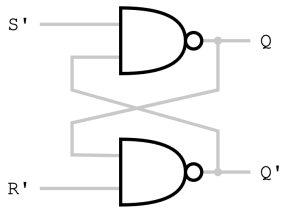
S' = R' = 0  	If both S' and R' are equal to 0, then both Q and Q' will want to be _____. This creates a _____.

Problem 2: Race Condition

The final values of Q and Q' are _____ when changing from

_____ to _____.

As previously stated, we cannot assume two signals can change at precisely the same time.

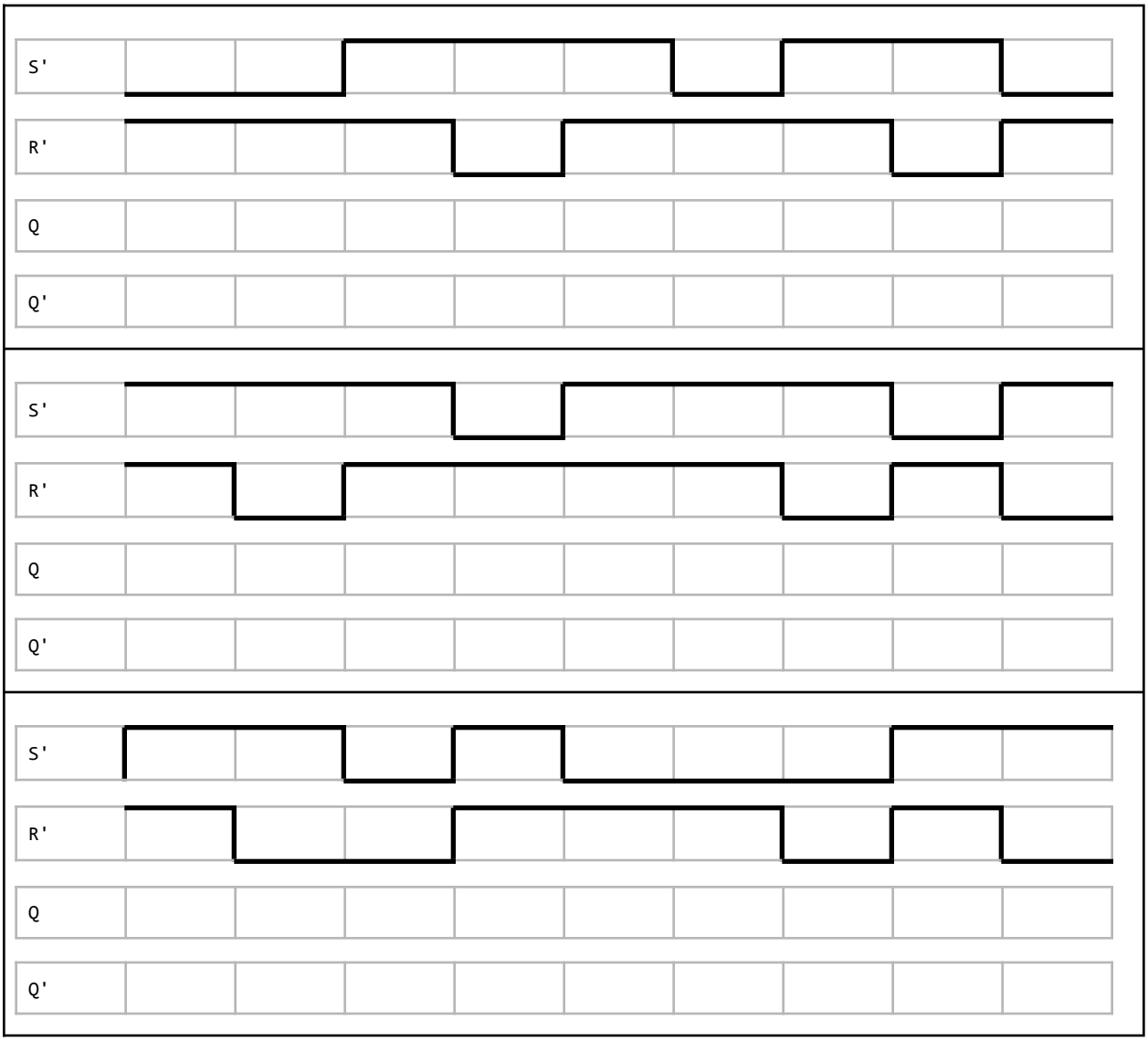
S' = R' = 1; Q_init = 1, Q'_init = 1; R' changes first  	If R' changes from 0 to 1 first, Q' will become _____ which will cause Q to become _____
S' = R' = 1; Q_init = 1, Q'_init = 1; S' changes first  	If S' changes from 0 to 1 first, Q will become _____ which will cause Q' to become _____

Summary

S'	R'	Q	Q'	Action
0	0			
0	1			
1	0			
1	1			

Active _____ S-R Latch Timing Diagrams

Fill out Q and Q' for given S' and R' signals.



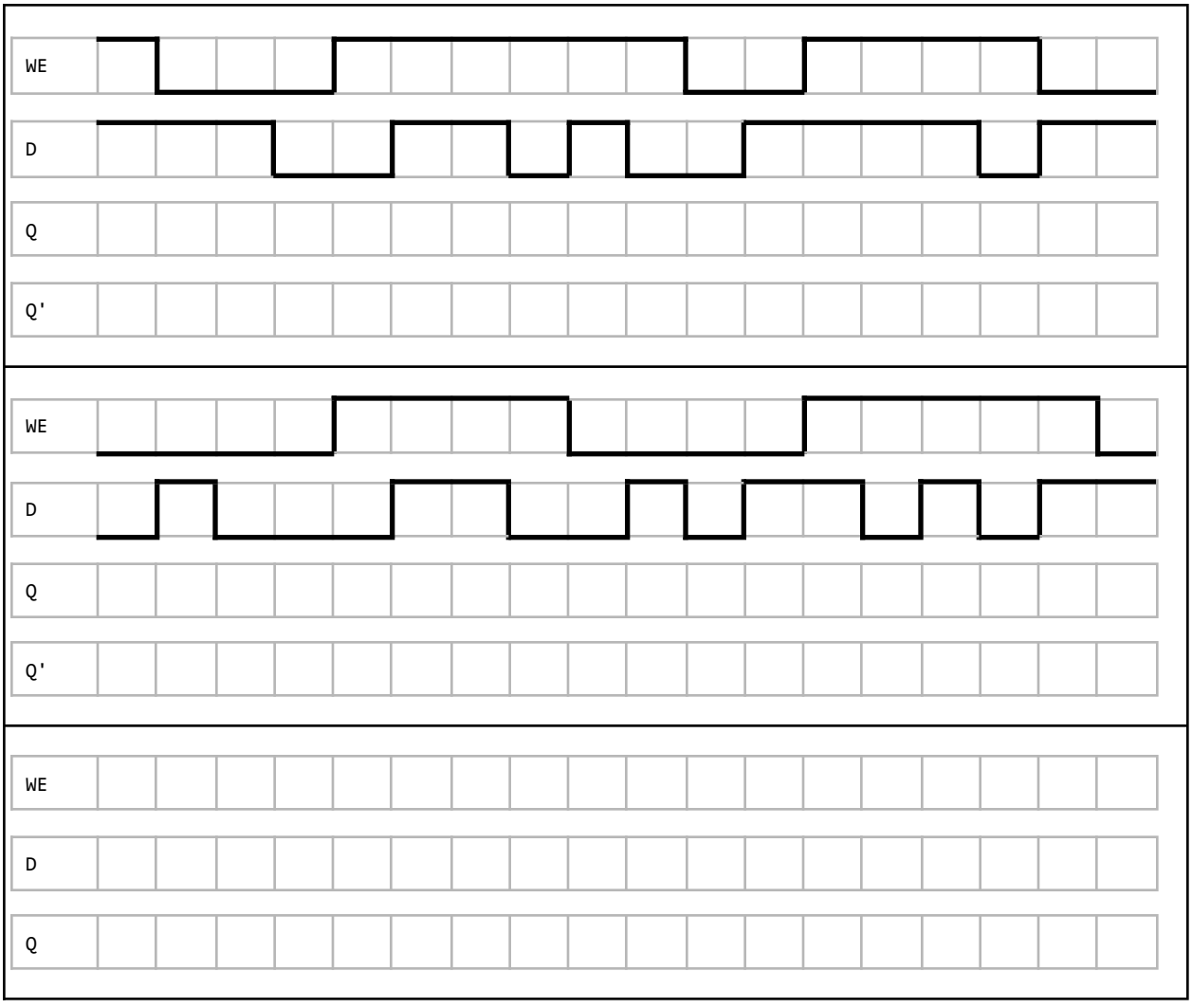
D Latch

Draw the schematic here:

WE	D	Q	Q'

Timing Diagram Examples

Fill out Q and Q' for given WE and D signals.



Register

A D latch is a device for storing _____. A _____ stores several bits.

Draw a diagram for a register:

Clock

The _____ for a signal to travel through a wire is _____.

For this reason, a _____ is used to _____ signals in a computer.

A clock is a free-running _____ signal

with a fixed _____.

The _____ of a clock is the _____.

Draw a clock signal. Label the rising edge, falling edge, and period.

CLK									

D Flip Flop

Flip flops are _____ sensitive.

_____ sensitive: the output changes on the _____ of the enable signal.

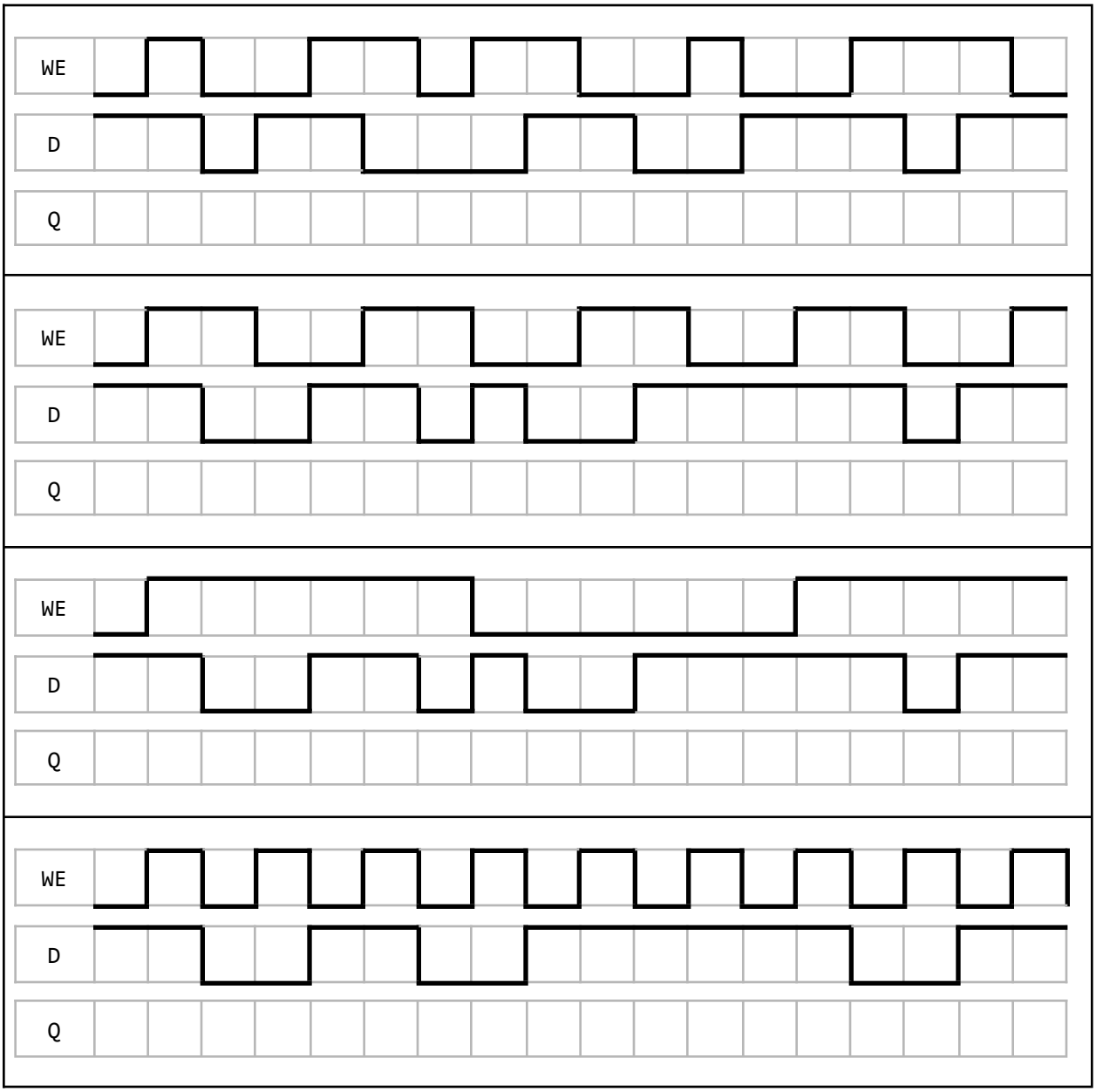
Positive Edge-Triggered Flip Flop

Draw the schematic here:

WE / CLK	Q	Q'
↑ 1		
other		

Timing Diagram Examples

Assume a positive edge-triggered flip flop. Fill out Q for given WE and D signals.



Negative Edge-Triggered Flip Flop

Draw the schematic here:

WE / CLK	Q	Q'
↓ 0		
other		

Timing Diagram Examples

Assume a negative edge-triggered flip flop. Fill out Q for given WE and D signals.